



RR-0821

Third Year B. Sc. (Electronics) Examination

March / April – 2010

Electronics : Paper - VIII

(Microprocessor Peripheral & Microcontroller)

Time : 3 Hours]

[Total Marks : 70

Instructions :

(1)

નીચે દર્શાવેલ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of signs on your answer book.

Name of the Examination :
T. Y. B. Sc. (ELECTRONICS)

Name of the Subject :
Electronics - 8

Subject Code No. : 0 8 2 1 Section No. (1, 2,.....): Nil

Seat No. :

Student's Signature

- (2) Figure on the right indicates full marks.
- (3) All symbols and abbreviations have their usual meaning.
- (4) Non-programmable calculators are allowed.
- (5) Q. 1 is compulsory.
- (6) Assume data if necessary.
- (7) Abbreviations have their usual meanings.

1 Answer in brief :

14

- (1) The memory of microcontroller is not shared between data and code where as Microprocessor has shared data and code memory. Why ?
- (2) Differentiate between microprocessor and microcontroller.
- (3) List the flags of 8051 and explain any one of them.
- (4) Why End of Interrupt signal is given twice in case of cascade mode of PIC operation ?
- (5) State the bit definition of PSW register of 8051.

(6) Explain the following instructions :

CPLA AND ANL A, @Rp

(7) State the similarities and differences between ALE pin of 8085 A and ADSTB of 8257 controller.

2 (a) Design a Chip Select generation scheme to interface one master and two slave 8259s in I/O Mapped I/O mode having following addresses : **7**

Master 8259 C0H C1H

Slave-1 C2H C3H

Slave-2 C4H C5H

Assume a buffered system environment. Draw a complete interface diagram. Slave-1 INT output must be connected to master IR 1 input. Slave-2 INT output must be connected to master IR2 output.

(b) Write an initialization routine for an 8259 (to be selected by addresses C0H and C1H) to set up for operation according to the followings specifications : **7**
Non-buffered system environment, normal EOI, 8085 A system, single 8259 operation, not in SFNM, CALL address internal equal to 4. First CALL address for IR0 must be F000H. Also, IR2 and IR3 must be masked.

OR

2 (a) How many instruction types are there in 8051 instruction set ? **4**

(b) What do you understand by addressing mode in 8051 ? **10**
How many addressing modes are there in 8051 ?
Explain all addressing modes in detail.

3 (a) Draw the functional block diagram of 8253 programmable Interval Timer and explain function of each block in detail. **6**

- (b) How many operating modes are available in 8253 ? **6**
 Explain any two in detail with suitable examples and clock diagram.
- (c) State the difference between 8253 and 8254 **3**
 programmable interval timer.

OR

- 3** (a) Write note on internal memory organization of 8051 **8**
 microcontroller.
- (b) Explain the bit definition of PCON register of 8051 **6**
 microcontroller. Explain in detail the power down mode and idle mode operation.
- 4** (a) State the control registers available in 8051 **5**
 microcontroller. Which control register will be useful in detection and initialization of interrupt in case of 8051 microcontroller ?
- (b) Explain any three controller register in detail. **9**

OR

- 4** (a) Write a program in 8051 to find minimum and **7**
 maximum value in an array of 8-bit numbers.
- (b) Write an 8051 assembly language program to convert **7**
 a 4-digit hexadecimal number to its equivalent ASCII. The 4-digit hex number is at internal RAM locations 30H and 31H. The equivalent ASCII is to be stored in four internal RAM locations starting from 50 H.
- 5** (a) Differentiate among DMA Write, DMA Read and **6**
 DMA Verify mode of operation of 8257 DMA controller.
- (b) Define each bits of Mode Set Register of 8257 and **8**
 explain rotating priority option, Extended Write option and TC Stop option of 8257 DMA controller in detail.

OR

- 5 (a) Write a program in 8051 to arrange an array in ascending/descending order. 7
- (b) Write an 8051 assembly language program to convert a 2-digit BCD number to its equivalent Binary value. The 2-digit BCD number is at external RAM location 200H. The result is to be stored in external RAM location 201H. 7
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